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Wafer-thickness dependence of double-side contacted rear junction *n*-type solar cells

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Abstract

We investigate the wafer-thickness dependence of double-side contacted rear junction *n*-type solar cells, theoretically by PC1D simulations and experimentally. To get the correct input parameters for PC1D, we first fit PC1D simulation to a rear junction cell fabrication of a complete ingot. The simulated cell performance of thin cells is mainly influenced by short circuit current J_{sc}. For wafer-thickness < 100 µm, light trapping becomes challenging and causes a steep decline in J_{sc}. This J_{sc} loss can also be seen in an IQE drop at long wavelengths of fabricated thin cells. For wafer-thickness > 100 µm, only minor variation in efficiency is predicted by simulation, which makes the cell concept suitable for 100 to 200 µm thick wafers. Median cell efficiencies of 20 % for 100 µm thin- 6" Cz Si cells are reported.

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Keywords: *n*-type silicon; wafer thickness; rear junction solar cell

1. Introduction

The wafer-thickness dependence of rear junction *n*-type solar cells is investigated in this article, theoretically by PC1D simulation [1,2] and experimentally. Thinner wafers are advantageous for saving Si material. The cell type is

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a double-side contacted rear junction *n*-type Cz Si solar cell with a 6 inch full square area. Front metallization is screen printing and rear metallization is through laser contact openings followed by Al-PVD (Fig. 1 left).

2. Fit simulation to experiment

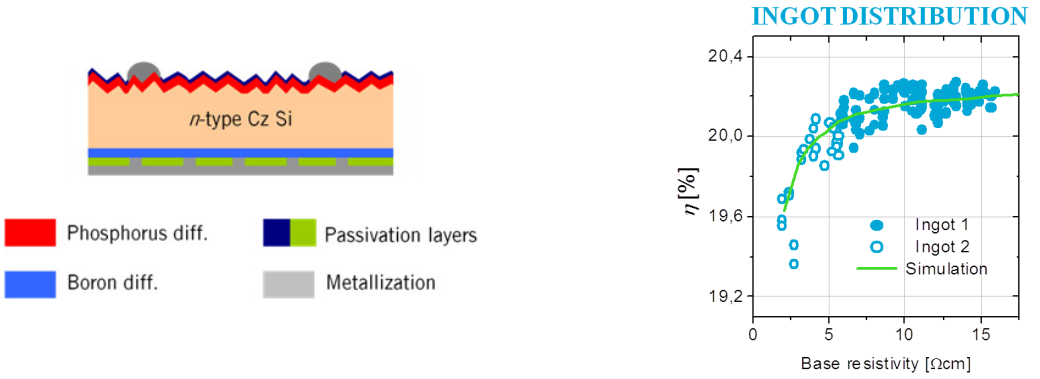

Fig. 1. Left: Cross section of the double-side contacted rear junction solar cell investigated within this article. Right: The cell results along an ingot distribution are fitted to obtain input parameters for PC1D.

We fitted our simulation to a rear junction cell fabrication along an ingot to obtain the correct input parameters for the PC1D simulation (Fig. 1 right). The PC1D simulation (green line in Fig. 1) with bulk lifetime independent of resistivity fits experimental data (bulk lifetime 3 ms, 160 µm thick wafer). This leads to the conclusion, that τ_{bulk} is limited by the solar cell process and thus independent of base resistivity [3]. Other input parameters for PC1D are:

- diffusion profiles for emitter and front-surface-field from SIMS or ECV
- Front reflectance including shading from metallization
- S_{front}: 8000 cm/s
- S_{rear}: 2000 cm/s

With these fit parameters it is possible to predict the influence of wafer thickness on rear junction cells.

The *n*-type ingot distribution is industrially feasible for complete ingots with > 5 Ωcm [3]. For the wafer thickness simulation we take the n-type-ingot resistivity distribution into account and simulate the cell performance of 5, 10, and 15 Ωcm base resistivity (Fig. 2 left).

3. Wafer thickness influence

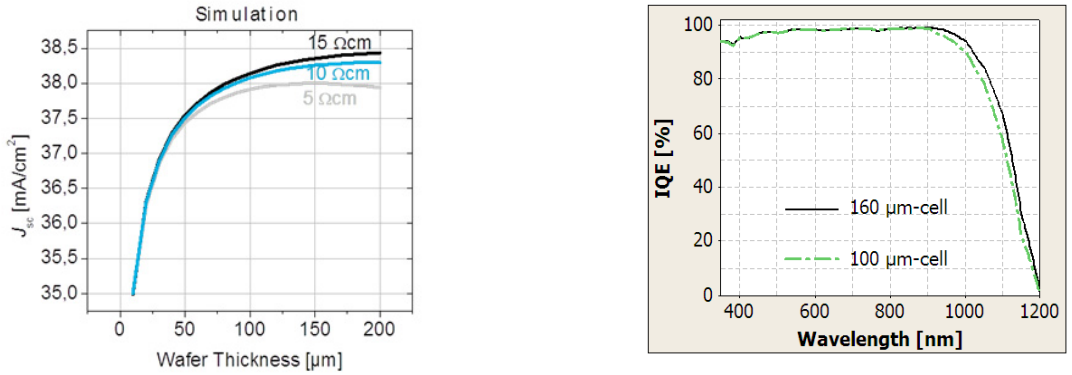

Fig. 2. Left: Insufficient light trapping causes steep decline in J_{sc} for wafer thicknesses < 100 µm. Right: 100 µm thin cells show an IQE loss for long wavelengths compared to 160 µm cells corresponding to the J_{sc} loss.

For wafer thicknesses < 100 µm the cell efficiency decreases strongly. This is caused by J_{sc} loss through insufficient light trapping (Fig. 2 left). The J_{sc} loss is experimentally confirmed and can also be observed in the long wavelength range of the IQE in Fig. 2 right.

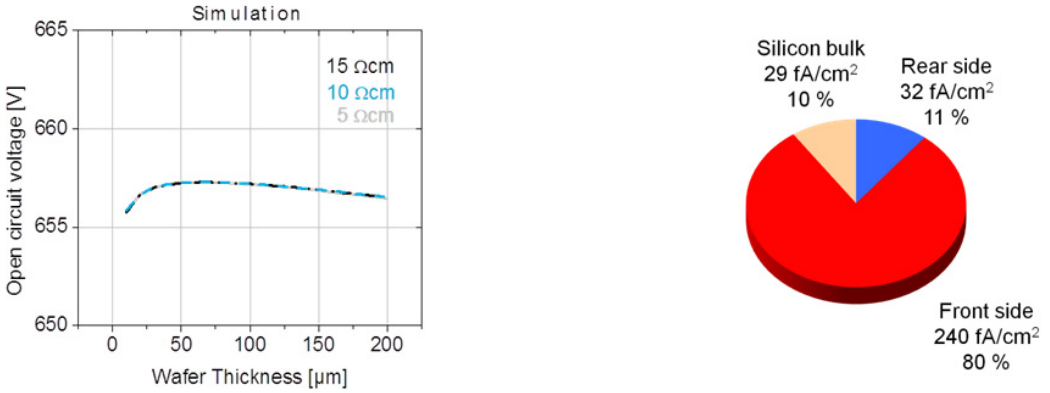

Fig. 3. V_{oc} increases only slightly for thinner wafers (left) due to small J_0 contribution of bulk (right).

In contrast to J_{sc}, the open circuit voltage varies only slightly in dependence of wafer thickness (Fig. 3 left) due to a small J_0 contribution of bulk (Fig. 3 right). Symmetrical lifetime samples of the front and rear design of the cell are produced to determine the front side and rear side J_0 contribution, that means samples with passivated diffused surfaces. The samples are measured with a Sinton tester [4]. The $J_{0,bulk}$ contribution is calculated for 10 Ωcm and 160 µm thick wafers in high level injection. Bulk contributes only 10 % to $J_{0,total}$ for rear junction *n*-type cells. High bulk lifetimes (> 1ms) of *n*-type material lead to the small $J_{0,bulk}$.

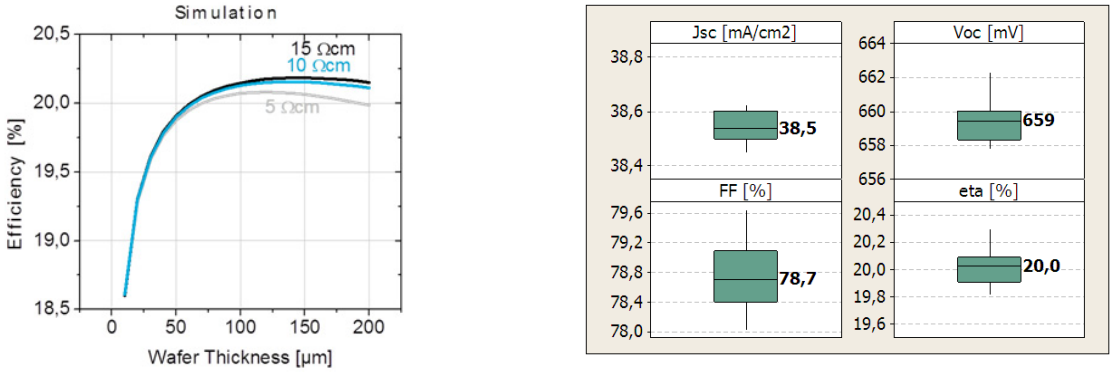

Fig. 4. Left: Simulated cell efficiency as a function of wafer thickness for different base resistivities. Wafer thicknesses between 100 and 200 µm result in highest efficiencies. Right: Measured cell parameters of 100 µm- thin cells: median cell efficiency of 20 % is shown.

The outcome of the simulation is: the rear junction cell concept is suitable for 100 to 200 µm thick wafers (Fig. 4 left). There is freedom of choice for wafer thickness > 100 µm, adaption to wafer market situation is possible. Figure 4 right shows the result of a 100 µm thin- 6" Cz Si cells fabrication. The median cell efficiency of 40 cells is 20 %.

4. Conclusions

The simulated cell performance of thin cells is mainly influenced by short circuit current *J*sc. For wafer thickness < 100 µm, light trapping becomes challenging and causes a steep decline in *J*sc. For wafer thickness > 100 µm, only minor variation in efficiency is predicted by simulation. This leads to the conclusion, that the rear junction cell concept is suitable for 100 to 200 µm thick wafers. Median cell efficiencies of 20 % for 100 µm thin- 6" Cz Si cells are reported.

Acknowledgements

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